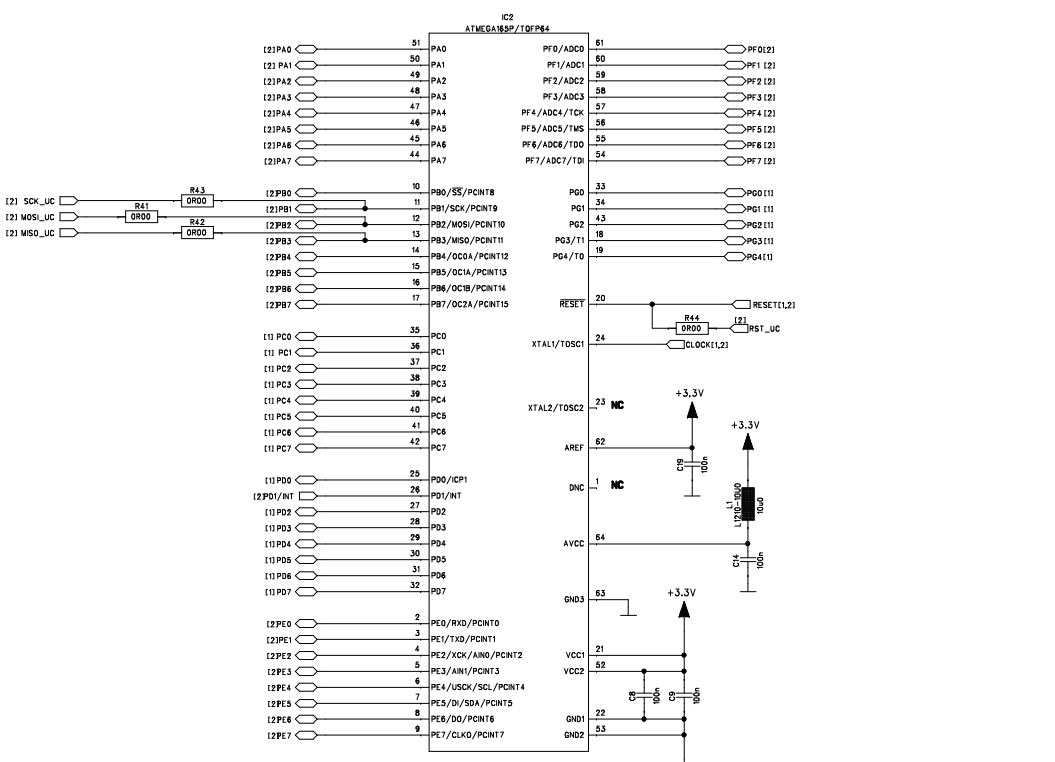
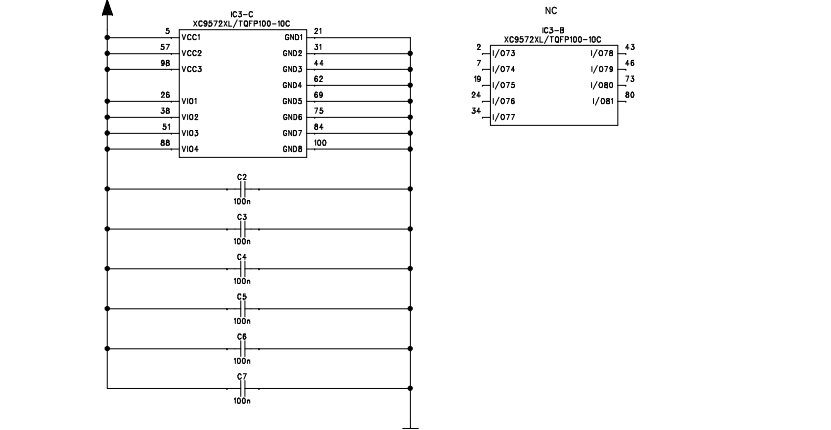
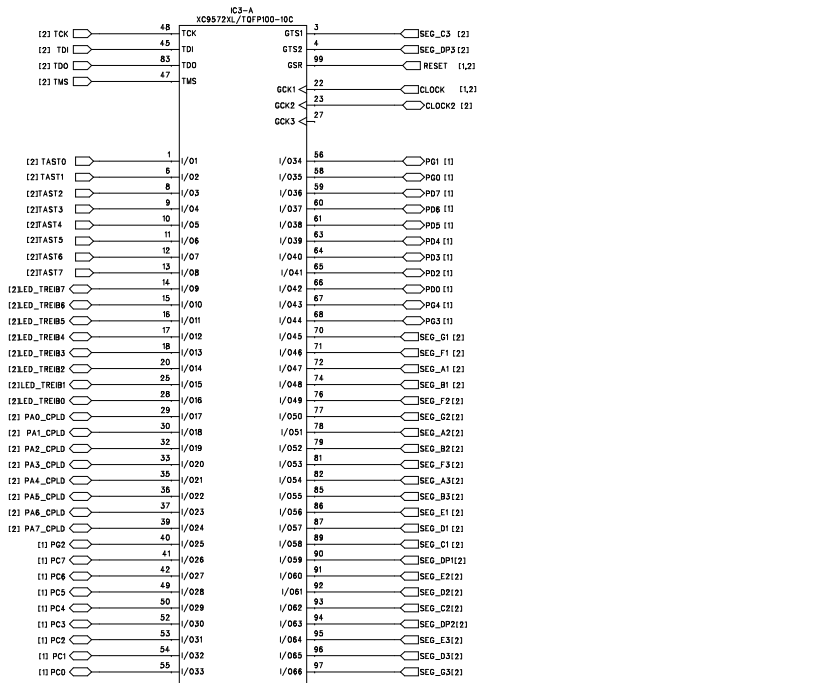


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REVISION RECORD			
LTR	ECCO NO:	APPROVED:	DATE:

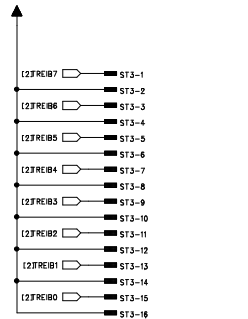
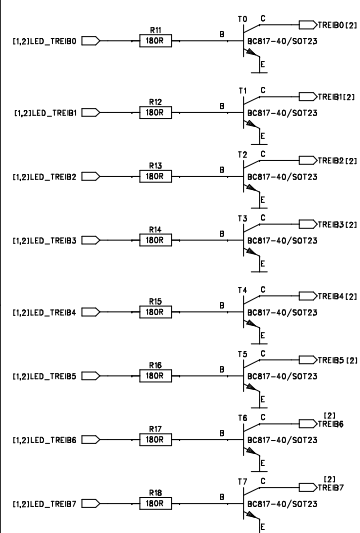


COMPANY:  
X2E GmbH

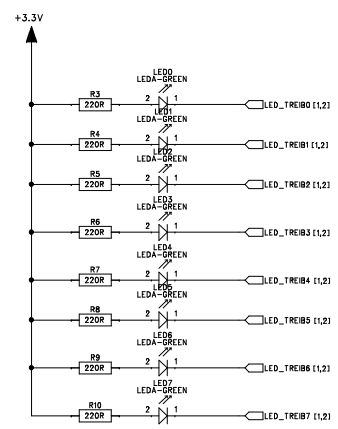
TITLE:  
Schulungsbaugruppe Programmierbare Logik Stufe 1

DRAWN: Michael Rapp, Michael Skinder	DATED: 16.07.2008	CODE:			SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:	SCALE:			SHEET: 1 OF 2		
QUALITY CONTROL:	DATED:						
RELEASED:	DATED:						

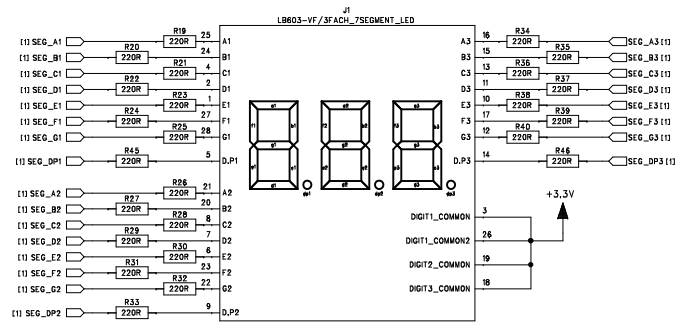
### Treiber



### LEDs

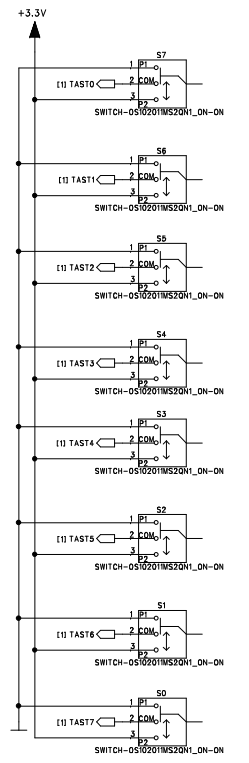


### Siebensegment-Anzeige

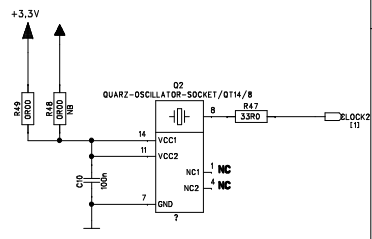


REVISION RECORD			
LTR	ECCO NO:	APPROVED:	DATE:

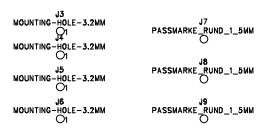
### Schalter



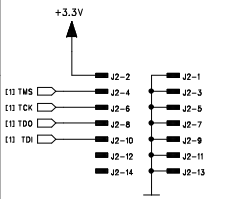
### Clock 2



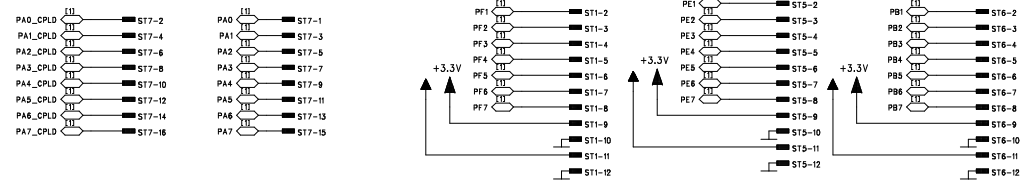
### Mechanik



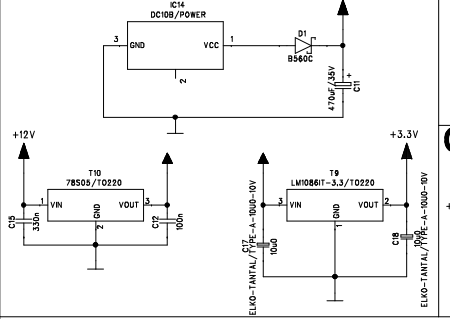
### CPLD prog.



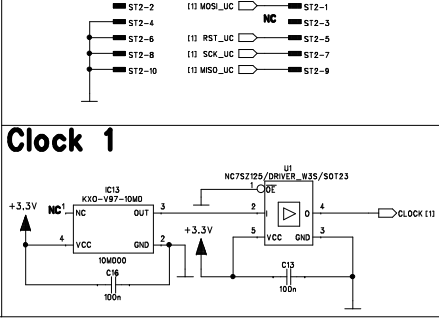
### uC-Ports



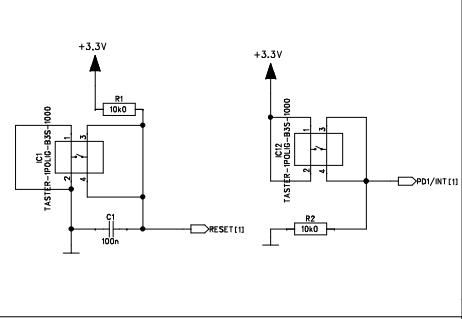
### Power



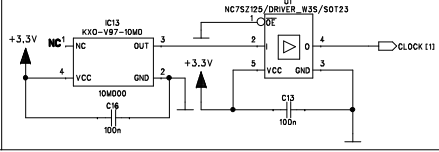
### Atmel prog.



### Reset, Int.



### Clock 1



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Michael Rapp, Michael Skinder	16.07.2008
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

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X2E GmbH			
TITLE:			
Schulungsbaugruppe Programmierbare Logik Stufe 1			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:		SHEET: 2 OF 2	